DATA SHEET

74LVC574A

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

Product specification
Supersedes data of 2003 Jun 20

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Philips
Semiconductors

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Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

74LVC574A

FEATURES

- 5 V tolerant inputs and outputs, for interfacing with 5 V logic
- Supply voltage range from 1.2 to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0 V
- 8-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Flow-through pin-out architecture
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC574A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC574A is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A clock (CP) and an Output Enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance off-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74LVC574A is functionally identical to the 74LVC374A, but has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Qn	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	15	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

OPERATING MODE	INPUT			INTERNAL FLIP-FLOP	OUTPUT
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
   ↑ = LOW-to-HIGH clock transition;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC574AD	–40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC574ADB	–40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC574APW	–40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC574ABQ	–40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	output enable input (active LOW)
2	D0	data input
3	D1	data input
4	D2	data input
5	D3	data input
6	D4	data input
7	D5	data input
8	D6	data input
9	D7	data input
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	CP	clock input (LOW-to-HIGH; edge triggered)
12	Q7	data output
13	Q6	data output
14	Q5	data output
15	Q4	data output
16	Q3	data output
17	Q2	data output
18	Q1	data output
19	Q0	data output
20	V_{CC}	supply voltage

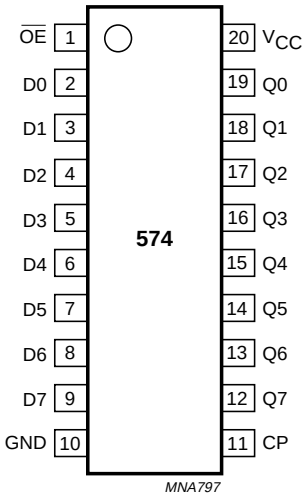
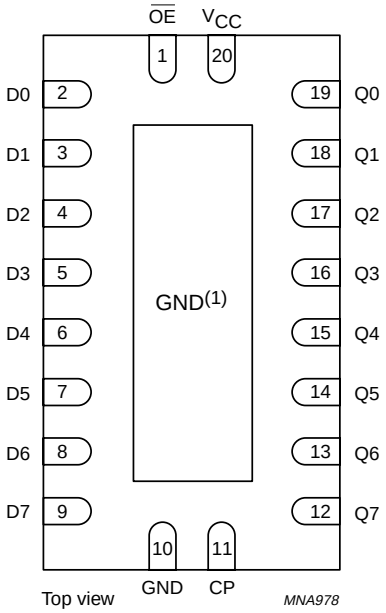


Fig.1 Pin configuration SO20 and (T)SSOP20.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN20.

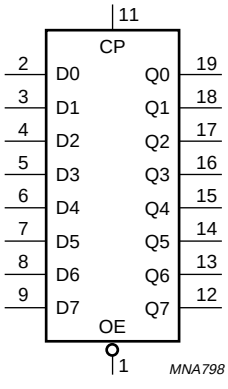


Fig.3 Logic symbol.

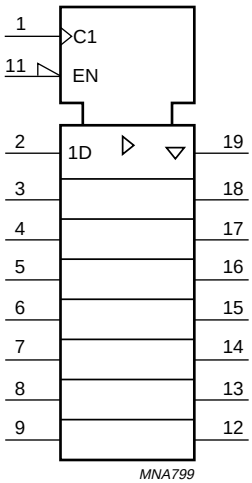


Fig.4 Logic symbol (IEEE/IEC).

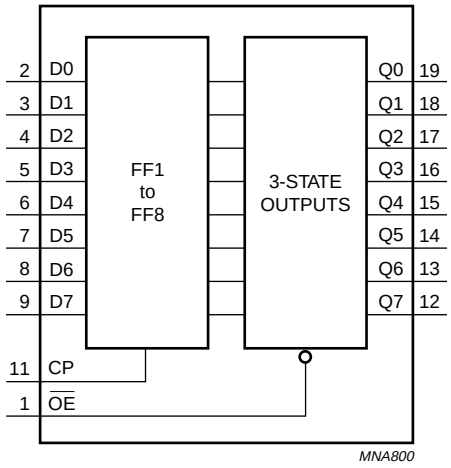


Fig.5 Functional diagram.

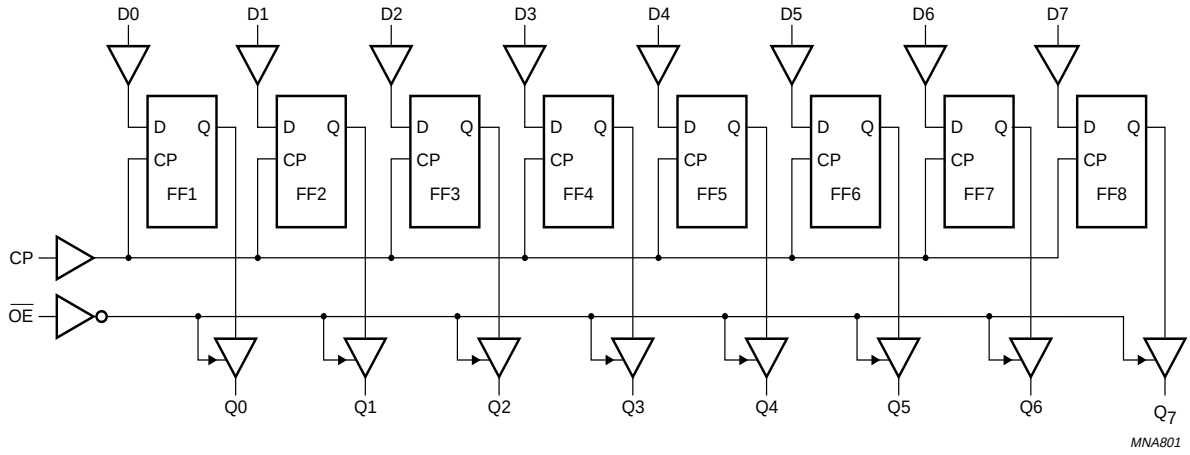


Fig.6 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		output 3-state; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
   For (T)SSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
   For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –12 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –100 μA	3.0	V_{CC} – 0.2	V_{CC}	–	V
		I_O = –18 mA	3.0	V_{CC} – 0.6	–	–	V
		I_O = –24 mA	3.0	V_{CC} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 12 mA	2.7	–	–	0.40	V
		I_O = 100 μA	3.0	–	GND	0.20	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6	–	0.1	±10	μA
I_{off}	power-off leakage supply	V_I or V_O = 5.5 V	0.0	–	0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0	2.7 to 3.6	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –12 mA	2.7	V_{CC} – 0.65	–	–	V
		I_O = –100 μA	2.7 to 3.6	V_{CC} – 0.3	–	–	V
		I_O = –18 mA	3.0	V_{CC} – 0.75	–	–	V
		I_O = –24 mA	3.0	V_{CC} – 1	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 12 mA	2.7	–	–	0.6	V
		I_O = 100 μA	2.7 to 3.6	–	–	0.3	V
		I_O = 24 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	–	±20	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6	–	–	±20	μA
I_{off}	power-off leakage supply	V_I or V_O = 5.5 V	0.0	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0	2.7 to 3.6	–	–	5000	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

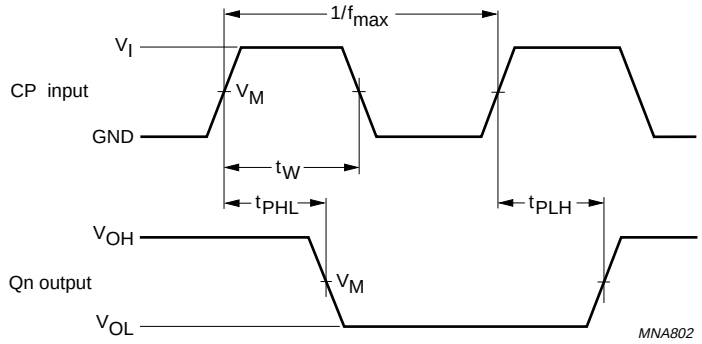
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	2.7	1.5	3.6	8.0	ns
			3.0 to 3.6	1.5	3.2[2]	7.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Figs 9 and 10	2.7	1.5	4.3	8.5	ns
			3.0 to 3.6	1.5	3.5[2]	7.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Figs 9 and 10	2.7	1.5	2.8	6.5	ns
			3.0 to 3.6	1.5	2.5[2]	6.0	ns
t_W	clock pulse width HIGH or LOW	see Fig.7	2.7	3.3	–	–	ns
			3.0 to 3.6	3.4	1.7[2]	–	ns
t_{su}	set-up time Dn to CP	see Fig.8	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0.3[2]	–	ns
t_h	hold time Dn to CP	see Fig.8	2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	−0.2[2]	–	ns
f_{max}	maximum clock frequency		2.7	80	–	–	MHz
			3.0 to 3.6	100	150[2]	–	MHz
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.0	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	2.7	–	–	10.0	ns
			3.0 to 3.6	–	–	9.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Figs 9 and 10	2.7	–	–	11.0	ns
			3.0 to 3.6	–	–	9.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Figs 9 and 10	2.7	–	–	8.5	ns
			3.0 to 3.6	–	–	7.5	ns
t_W	clock pulse width HIGH or LOW	see Fig.7	2.7	–	–	–	ns
			3.0 to 3.6	–	–	–	ns
t_{su}	set-up time Dn to CP	see Fig.8	2.7	–	–	–	ns
			3.0 to 3.6	–	–	–	ns
t_h	hold time Dn to CP	see Fig.8	2.7	–	–	–	ns
			3.0 to 3.6	–	–	–	ns
f_{max}	maximum clock frequency		2.7	–	–	–	MHz
			3.0 to 3.6	–	–	–	MHz
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	–	ns

Notes

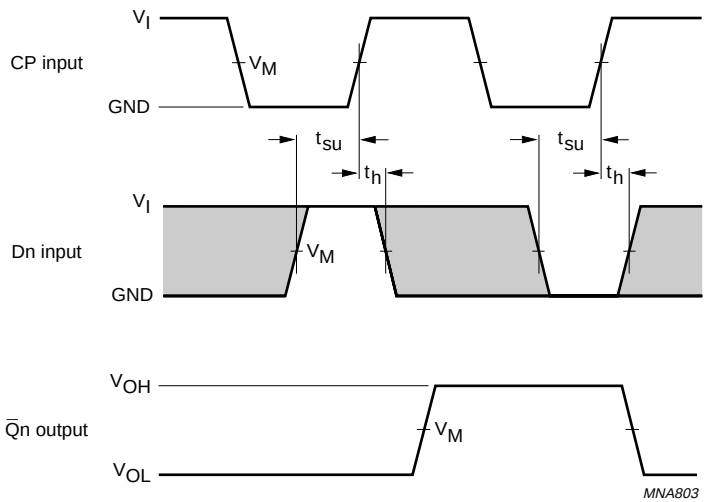
1. All typical values are measured at $T_{amb} = 25$ °C.
2. These typical values are measured at $V_{CC} = 3.3$ V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



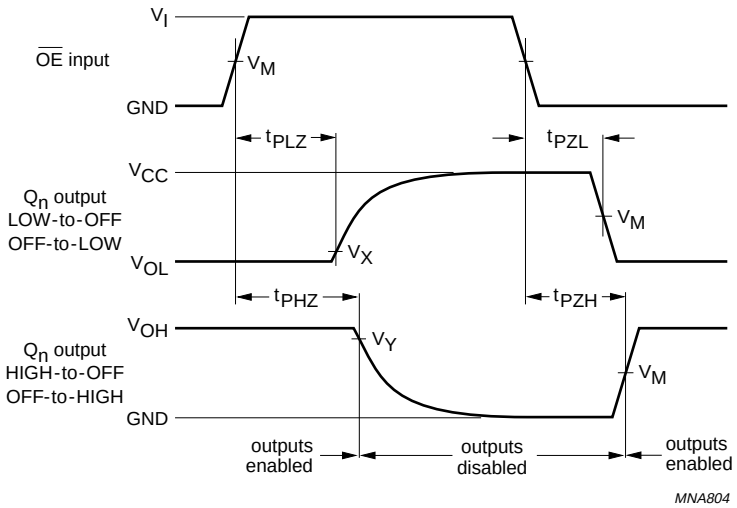
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
V_M = 0.5 V_{CC} at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig.7 Clock (CP) to output (Qn) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



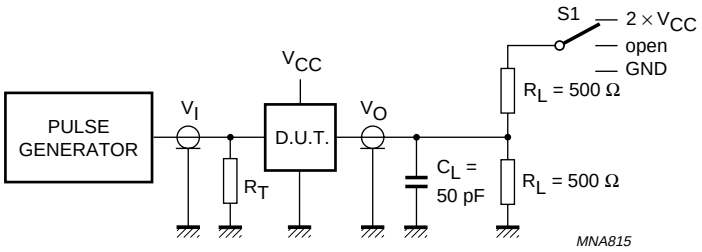
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
V_M = 0.5 V_{CC} at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.8 Data setup and hold times for the Dn input to the CP input.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq$ 2.7 V;
$V_X = V_{OL} + 0.1V_{CC}$ at V_{CC} < 2.7 V.
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V;
$V_Y = V_{OH} - 0.1V_{CC}$ at V_{CC} < 2.7 V.

Fig.9 3-state enable and disable times.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

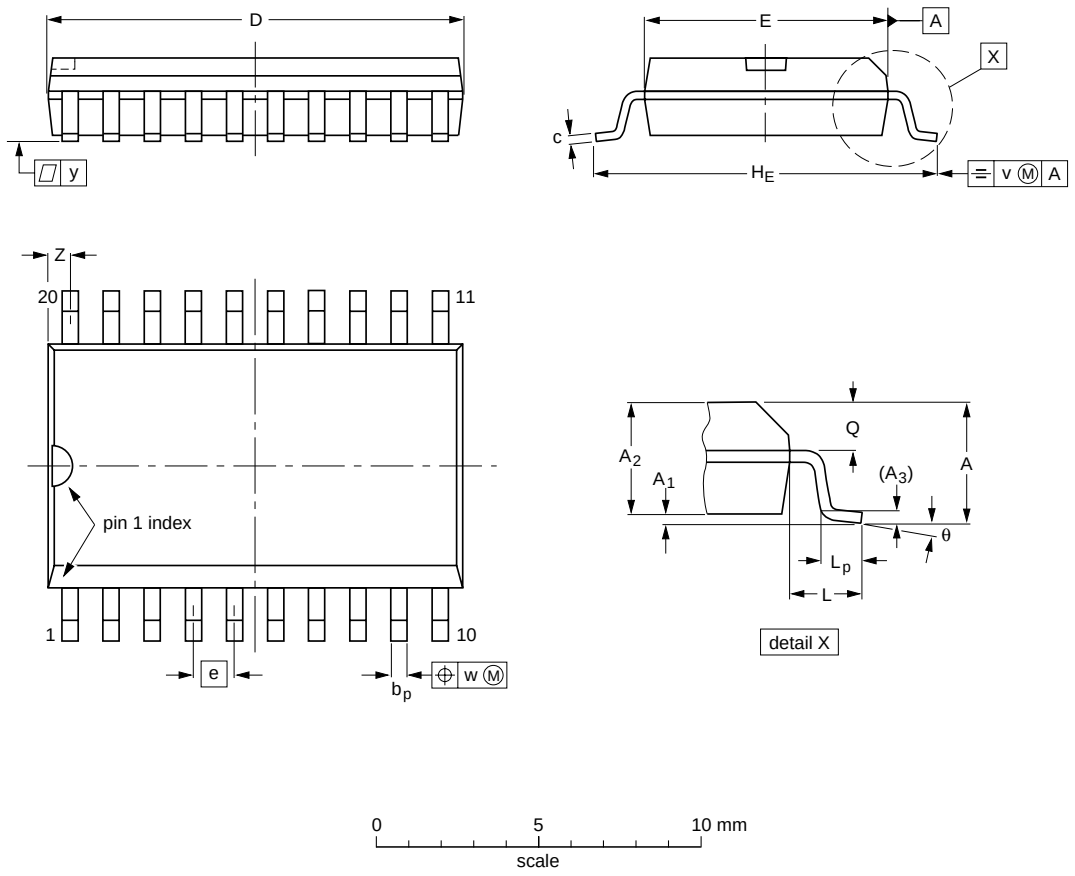
V_{CC}	V_I
<2.7 V	V_{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuit:
R_L = load resistor.
C_L = load capacitance includes jig and probe capacitance.
R_T = termination resistance should be equal to Z_o of pulse generators.

Fig.10 Load circuitry for switching times.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

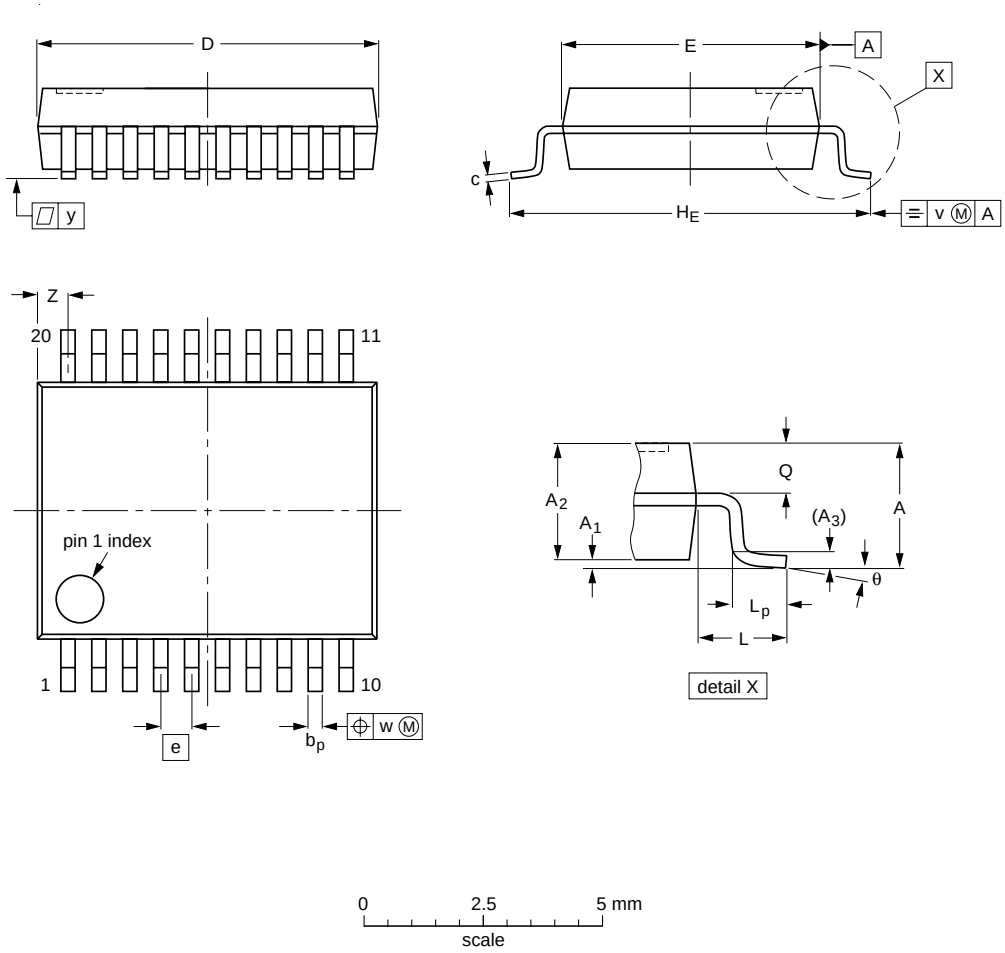
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

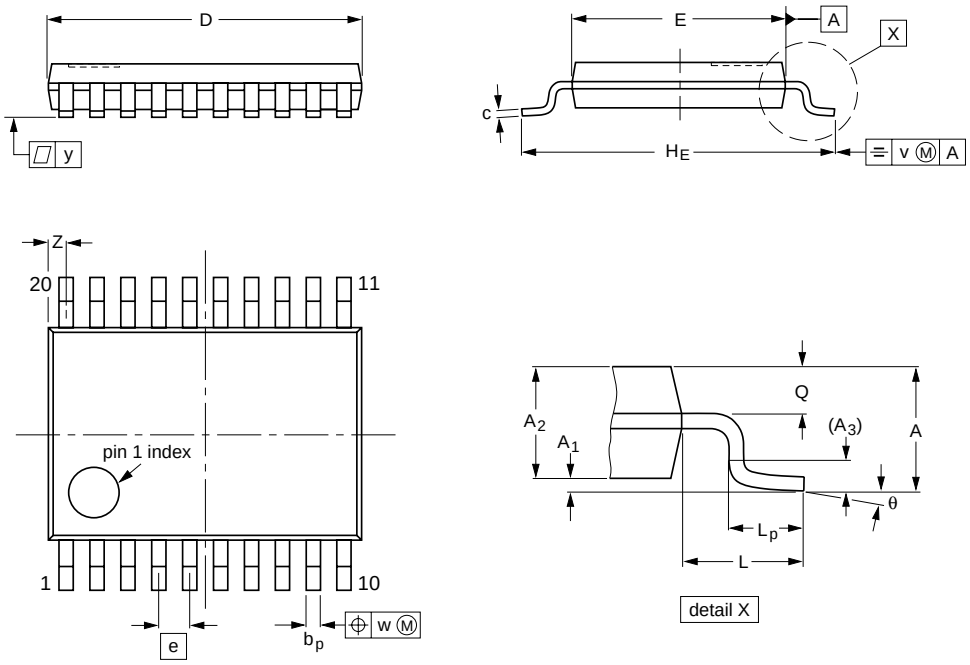
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

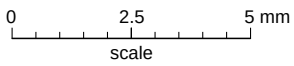
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

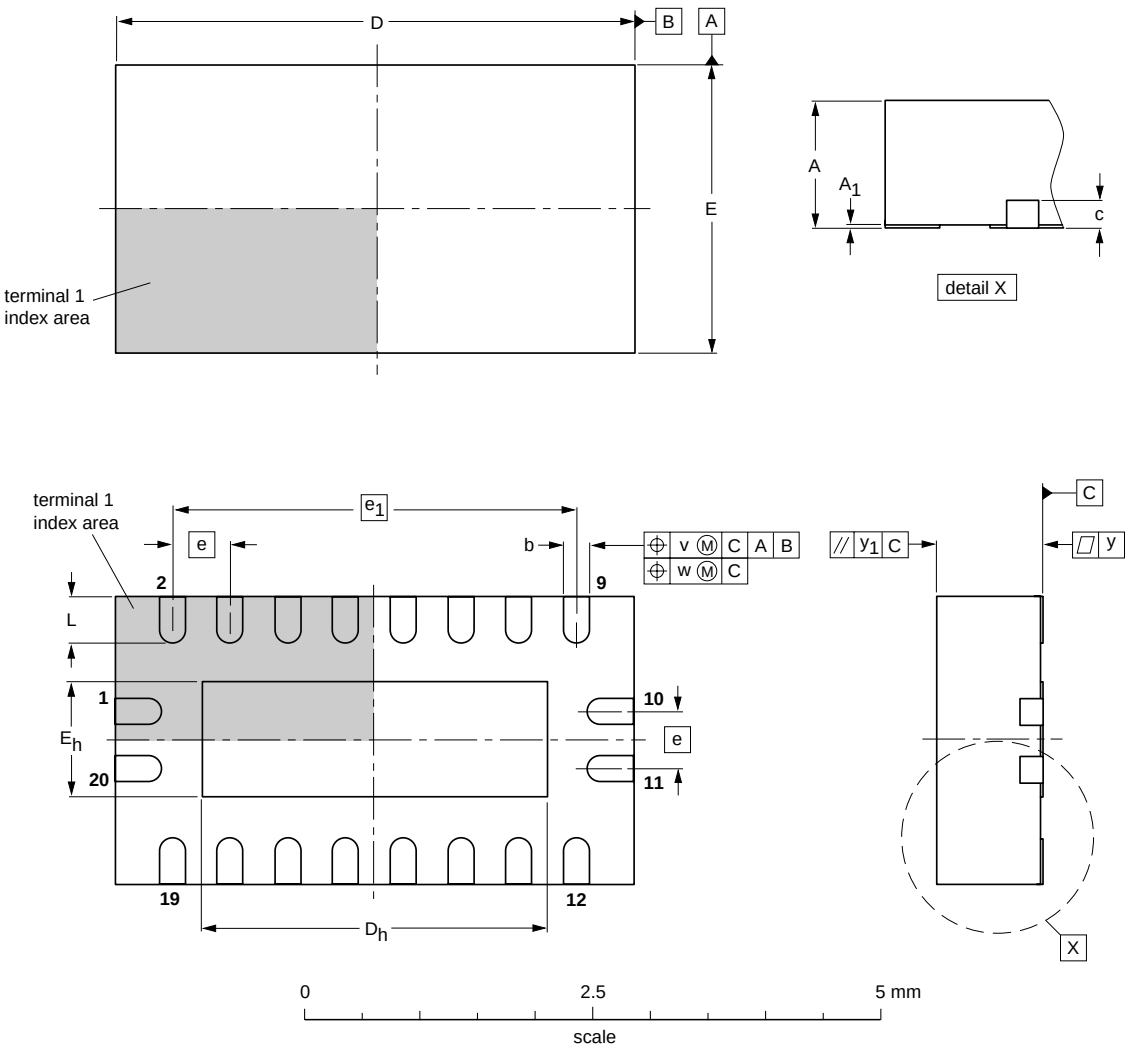
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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